

SOC DESIGN OFTEN INCLUDES ANALOG AND MIXED-SIGNAL CIRCUITS.

UNDERSTANDING SOME OF THE CHALLENGES OF THESE DEVICES

HELPS ENGINEERS DEVELOP A SUCCESSFUL SOC-DESIGN STRATEGY.

Designing analog and mixed-signal circuits on digital-CMOS processes

CMOS WAS DEVELOPED AS A DIGITALLY friendly process. Now, thanks to high levels of system integration and the emergence of SOC (system-on-chip) design, CMOS has also become the process of choice for mixed-signal applications. However, cutting-edge CMOS has limitations in these applications. Process restrictions, inaccurate simulation models, wide parametric variance, and noisy application environments require special efforts in circuit design, architecture, and layout techniques and in making optimal use of a limited process. Addressing these issues provides a system-development strategy for mixed-signal circuitry on CMOS.

A DCP (digital-CMOS process) optimizes logic functions, including switching speed, low-voltage power supplies, submicron geometry, and high component density. Considerations that address analog and mixed-signal circuits are not emphasized in the definition of process parameters. Full process characterization and analog-circuit elements get left out.

High CMOS volumes and the preference for digital-signal-processing methods motivate engineers to seek viable CMOS-SOC designs. Bipolar and other non-CMOS processes now find use primarily in applications that require special performance characteristics. To implement successful mixed-signal designs, you must use several strategies to get the most out of a restrictive process, reduce noise, use design techniques for process and environment robustness, and decide between digital and analog architectures. You must develop strategies for circuit elements and their models, circuit architecture, layout, and mask design.

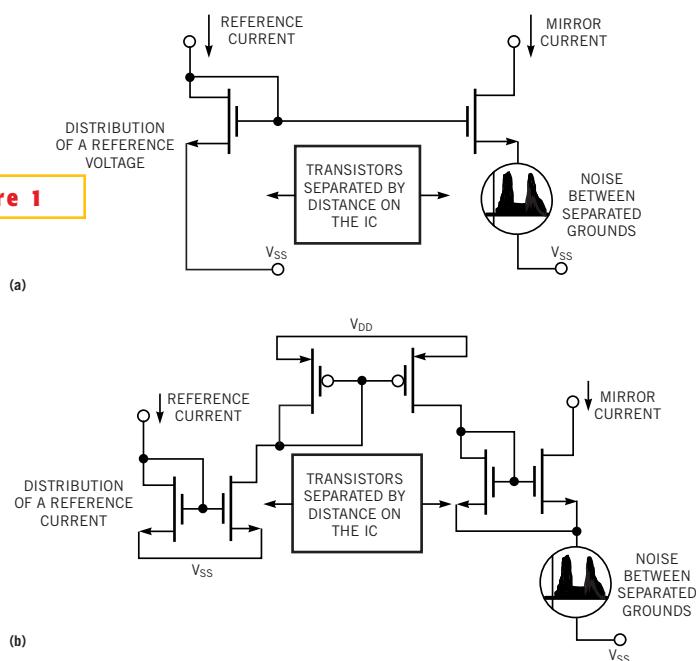
CIRCUIT ELEMENTS AND THEIR MODELS

Moore's law dictates that CMOS processes quickly shrink; this situation requires rapid process-de-

velopment cycles to be necessary. Developing a CMOS wafer process typically involves simulating wafer fabrication and lithography, extracting parameters from the simulation, and developing preliminary models based on extracted data. Circuit designers get inaccurate models, and so using those models results in accuracy problems. Digital design is less sensitive to accuracy than analog circuits, so using simulations based on other simulations is practical only for all-digital ASICs.

A DCP restricts the process to those elements

Figure 1



To distribute bias control, designers typically distribute either the reference voltage (a) or the reference current (b). Distribution of a reference voltage can lead to a large amount of current modulation in the current mirror due to variations between grounds.

necessary for logic design. A full set of bipolar elements is unavailable; resistor structures are limited to process layers used in CMOS transistors. Mixed-signal CMOS frequently adds a second polysilicon layer for resistors or polysilicon-to-polysilicon capacitors. Limited-performance bipolar elements are also possible. Foundries frequently base their DCPs on extracted methods. After proving the process in digital-only applications, they implement a derivative process with a second polysilicon layer. This approach improves model accuracy because the foundries base their models on silicon, not process simulations.

The accuracy and detail of characterization data often determine whether you can successfully design mixed-signal circuits on a process. If you have detailed and accurate data, you can often develop circuits to work around the restrictions of the process.

In a process-characterization report, you should check whether capacitor models have parasitic elements that cause substrate coupling. These elements include both “bottom-plate” to the substrate and “top-plate,” or fringe, effects. Resistors also have capacitance to the substrate and change in value over process, temperature, and geometry variations. Resistors made from diffusions can vary as a function of the dc bias to the substrate.

Transistors have variation in threshold voltages, or drain current, between devices. You need to carefully analyze matching of elements of a common wafer. Parametric variance is generally

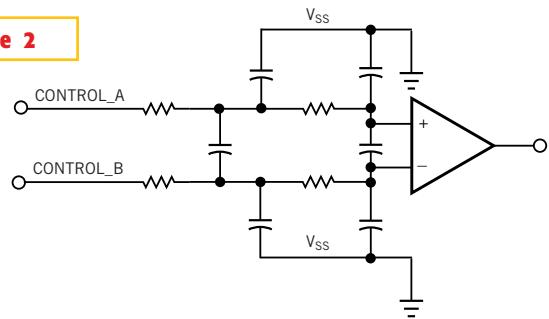
higher for smaller geometry devices. Performance degeneration due to short-channel effects, threshold variance, and body effect needs accurate models.

Due to differences of elements across multiple wafers and fabrication cycles, data on process variation should be made available. For example, resistors can vary by 20%, and transistors on some wafers can be weaker than on others. You must account for and include these nonideal characteristics in your simulations. If you have no accurate data, the probability of a successful design decreases.

Ideally, when selecting a process for mixed-signal design, the process characterization should include parameters and statistical variance for all elements, matching data of elements over a wide range of sizes, capacitor parasitics and leakage, resistor models with parasitics and variance due to bias and temperature, pnp bipolar models, and CMOS-transistor models and their weak/strong variance.

A need exists for circuit elements that DCPs do not normally use. You can design low-performance pnp transistors on N-well CMOS processes. Designers have used these devices in Gilbert-cell multi-

Figure 2



NOTES:
SPECTRAL CONTENT OF "CONTROL A/B" IS BELOW THE FILTER'S FREQUENCY AT WHICH IT STARTS TO ATTENUATE. SWITCHING NOISE, NORMALLY HIGH-FREQUENCY, IS PREVENTED FROM ENTERING THE AMPLIFIER.

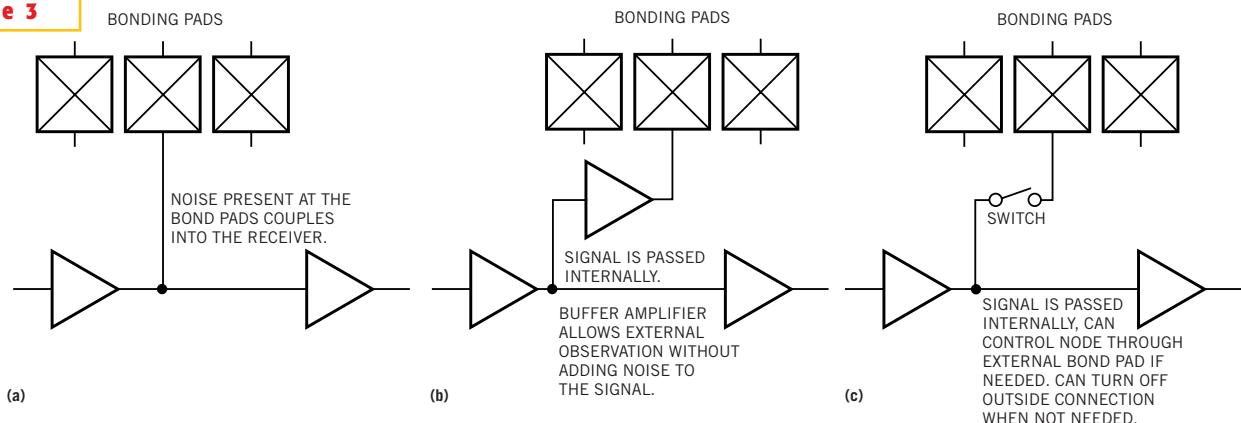
A common implementation provides both differential and common-mode filtering relative to the local ground.

pliers and matched pairs in differential amplifiers. Although pnp collectors are tied to the substrate, they are also suitable for bandgap references. Capacitor structures are available from the gates of CMOS transistors or adjacent metal-layer capacitors. You can develop substrate-tied capacitors using diffusions and isolation wells to the substrate. For processes having two polysilicon layers, designers frequently use these layers for capacitors.

POWER, THRESHOLDS, AND CIRCUIT BIAS

As CMOS gets smaller, gate oxides become thinner, and power-supply voltages consequently decrease. State-of-the-art CMOS now requires less than 2.5V. However, analog circuits frequently require three to five transistors, connected drain to source, between power and ground. Threshold voltages restrict the number of

Figure 3



Avoiding off-chip noise coupling: You can connect signals to an external pin, but this approach causes signal noise (a). In another approach, you can pass the signal internally and use a buffer amplifier to allow external observation (b). Another approach allows external observation and the ability to connect to the internal node (c). Digital control allows isolation from external noise if the pin is not in use.

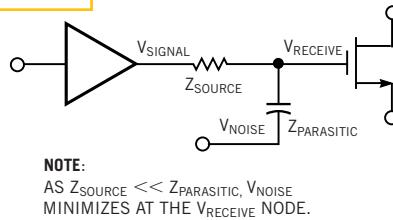
transistors that can be properly biased. A higher supply voltage is sometimes viable. However, small-geometry processes have low breakdown voltages and thin gate oxides, restricting the power supply. Consequently, having sufficient voltage headroom in analog-circuit designs can be problematic.

When CMOS power several years ago decreased to less than 5V, I/O cells that would connect to external 5V logic became necessary. Some foundries introduced dual gate oxides to allow 5V I/O compatibility, and designers of mixed-signal circuits quickly used this two-oxide technology to produce 5V-compatible circuits.

TRANSISTOR-ARRAY DESIGNS

Some DCPs use transistor-array, or gate-array, architecture, which uses a unique set of metal layers to define circuitry. Analog designs on gate-array processes can present problems, because layout is restrictive. However, the technique is successful in some applications. One restriction of gate arrays are their fixed transistor geometry. However, you can design variable channel widths and lengths using transistors in parallel and series. Distributed capacitance in the layout can degrade performance. Designs with transistor arrays have greater success at lower frequencies and in applications in which transistor mismatch is not critical. However, selective layouts, shielding, and noise-isolation efforts are often not viable on these devices. The use of transistor-array designs do not allow optimal designs. Designs that can gener-

Figure 4



Lower impedance circuits generally have better noise immunity.

ate custom layouts are preferred.

Another factor, the ground reference across an IC, has dynamic variance due to substrate currents and inductance of the connections. This situation results in noise from switching transients between grounds across the IC. The presence of noise dictates many of the strategies designers use on these ICs. To distribute bias control, designers typically distribute either a reference current or a reference voltage. Small induced voltages can lead to a large amount of current modulation in a current mirror (**Figure 1**). Distribution of a bias current across the IC avoids current source modulation. Bias distributed as a current enters the diode-connected device, which connects to the local reference ground. This technique provides a local voltage reference for control of the current source.

STABLE POWER SUPPLIES

Digital switching causes RF noise on the power supply. The impedance of power and ground connections is inductive, causing both ground bounce

and noisy power. Designers prefer to use isolated power supplies for analog circuits. They also use internal voltage regulators in special cases. Power supplies are sometimes noisy because of internal noise coupling. Some noise is present on all nodes, and a multitude of techniques exists to reduce the net effect of this noise. These techniques include architecture inside the IC, circuitry outside the IC, and die layout inside the IC.

Because noise coupling is distributed, isolation and filtering, to be effective, also need to be distributed. This approach involves filtering both the power and the signal/control nodes. Low-frequency power filtering can be external to the IC.

You should determine the frequency at which external filter capacitors become ineffective. Due to physical structure, all capacitors have reactive components that cause variance from an ideal response. Inductive resonance of ceramic surface-mount capacitors is due to a series LC circuit. Above resonance, inductance dominates the impedance of the capacitor, and the capacitor becomes an ineffective filter. Distributed values of filter capacitors allow resonance points to overlap, minimizing self-resonance effects (**Reference 1**). External filters need to be close to the IC to minimize inductance of the pc-board connection.

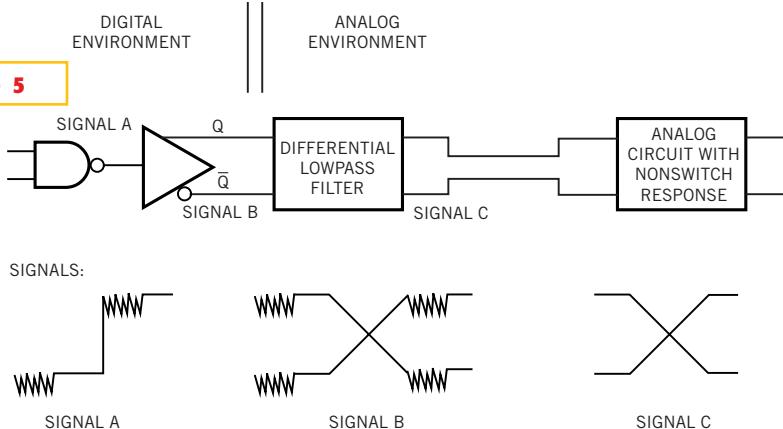
Logic with rise and fall transients of picoseconds leads to RF spectral noise that defies external filters. The IC package and bond wire have inductance that degrades the performance of external filters at high frequencies.

In these cases, you need to place capacitors on the die for high-frequency filtering. Power filtering for devices that use constant or low currents may benefit from RC sections between the power supply and the circuit. This approach provides a quieter power source. You should review whether you can afford to lose voltage headroom due to the filter or tolerate voltage variations due to current surges.

QUIET SIGNALS

In addition to power filtering, the use of filters on control signals reduces noise. A common implementation provides both differential and common-mode filtering relative to the local ground (**Figure 2**). The spectral response is ineffec-

Figure 5



You can pass digital control into an analog environment with minimal noise effects.

tive within the control-signal bandwidth yet provides attenuation for the clocking frequencies of the logic. In this case, active filters are ineffective because high-frequency noise can couple through their parasitic capacitances. Passive RC filters, on the other hand, are simple to implement and effective in reducing RF-digital-switching noise.

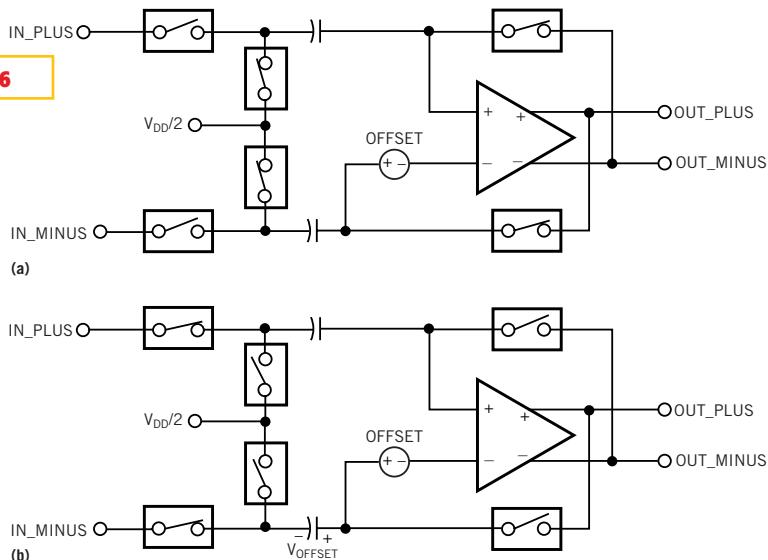
Systems operating in noisy environments benefit from using differential signals to reduce noise coupling. Differential signals between stages with the lines routed together have common-mode noise, which the receiver can reduce. Fully differential circuits also reduce the effects of power and ground noise. Most analog designs are differential within the chip. Any external ground-referenced signals usually change to differential signals upon entering the IC.

However, signals going outside the IC usually have increased noise coupling. Any noise-sensitive signal should have a minimal amount of routing. You frequently need to observe, not control, these signals. In these cases, you can pursue other methods to avoid off-chip noise coupling. Passing the signal off-chip incurs certain problems (Figure 3a). Coupling external noise to the pin causes signal noise. Passing the signal inside the IC and using a buffer amplifier allow external observation (Figure 3b). If necessary, you can connect to the internal node with a switch (Figure 3c). However, digital control allows you to isolate the node from external noise if the observation pin is not in use. These methods improve noise performance and let you control and observe the signal.

Connections outside an IC have better noise immunity with large amplitude signals to achieve the desired control. Small-amplitude input signals that require high gain have better performance in a dedicated, all-analog low-noise amplifier or preamplifier. High-gain-input circuits can also be noise-sensitive. Common examples of these circuits include the inputs of op amps and comparators. Op-amp inputs should remain inside the IC when possible. Comparators can be bandwidth-limited or include hysteresis in the design for noise immunity.

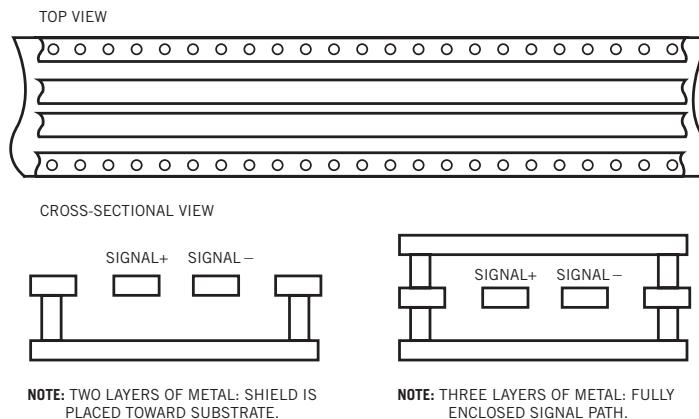
High-impedance nodes are more susceptible to noise coupling. Most MOS circuits use gates of transistors as ampli-

Figure 6



Dynamic offset compensation: When the comparator is in precharge mode, the capacitors' inputs connect to a common voltage, and outputs are fed back to drive the coupling capacitors (a). When the comparator is in compare mode, the input connects to the comparator through a capacitor voltage that cancels the input offset voltage (b).

Figure 7



NOTE: TWO LAYERS OF METAL: SHIELD IS PLACED TOWARD SUBSTRATE.

NOTE: THREE LAYERS OF METAL: FULLY ENCLOSED SIGNAL PATH.

You can achieve additional noise isolation in metal-mask design by using shielding on all sides that is electrically connected by vias and grounded.

fier inputs. High-impedance gate inputs are prone to noise coupling. In these cases, you should review the impedance of the circuit that drives the gate. Lower impedance circuits generally have better noise immunity (Figure 4).

Some digital controls must pass into and out of the analog part of the IC. How much isolation is necessary depends on the application. Some linear systems must remain functional while digital controls change, requiring some signal processing to avoid transient switching noise in the analog section. A multistage-

isolation method works reasonably well (Figure 5). The slew rate limits control signals and provides a differential output. You can insert a differential filter with low bandwidth and reference it to the analog power supply.

Make sure that the receiver takes the “soft-switched” control and responds linearly. Input to a comparator would immediately generate more switching noise. This technique passes the digital control into the analog environment with minimal noise. The approach routes the outputs of the differential control as a pair,

so transients are complementary, and provides a minimal noise source.

BANDWIDTH-LIMITING

Linear circuits with proximity to digital signals require designs that do not respond to switching noise. You should design active-gain stages with a spectral response suitable only to the signals of interest. Many designs include circuits with bandwidth above the desired signal. Although you can eliminate noise by bandwidth-limiting or filtering just the output circuits, this approach causes noise propagation and distortion among internal circuitry. Bandwidth-limiting of amplifiers offers the added bonus of power reduction, due to the lower currents that frequency-response reduction uses.

ANALOG OR DIGITAL ARCHITECTURE

DCPs are evolving rapidly with shrinking logic transistors, reduced threshold voltages, and lower power-supply voltages. At the gate level, synchronous digital designs are largely immune to these changes, whereas analog circuitry is not. When moving an analog design between processes, you must fully analyze and revalidate the design. Digital designs allow easier portability between processes. Further, digital has become largely automated, based upon functional definition in an HDL. Analog designs, on the other hand, still require a large amount of manual validation and analysis.

Choosing whether to use an analog-circuit or a digital-circuit architecture depends largely on the design's ability to convert the signal. If the design can perform acceptable analog-to-digital and digital-to-analog conversion, digital-signal processing can usually provide a suitable transfer function. Accuracy and sampling rates of converters become the limiting factors of this strategy. Analog-signal processing is more susceptible to noise and process variances. Digital implementations, though frequently more complex, often use a smaller die area. Consequently, DACs and ADCs are important design components, and they must be accurate on a process that can

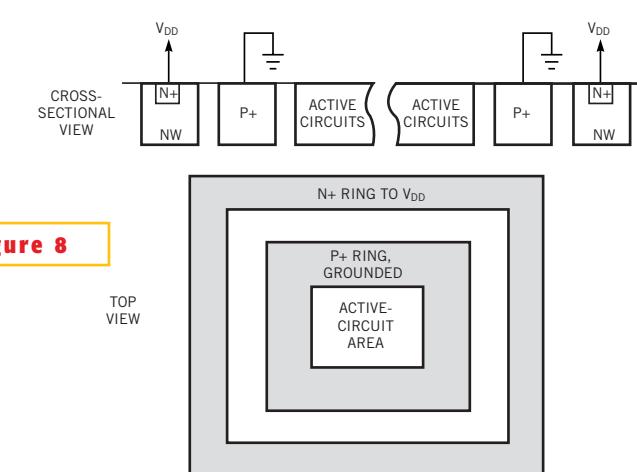


Figure 8

A grounded guard ring uses a low-resistance P+ area to connect to ground. A guard ring that connects to the power uses an N-well and N+ region on the substrate.

have a large amount of variance. Using a digital-control system to calibrate and align the analog parts of the system can be a powerful tool to compensate for the process variances you encounter.

Junction-mismatch effects manifest themselves as offsets in amplifiers and as imprecise current-mirror matching. Circuit mismatches are more problematic in CMOS because it has larger threshold-voltage variance than bipolar base-emitter junctions. Process control in DCPs can tolerate wide variances and produce acceptable digital circuits; analog requirements are more stringent. Larger geometry elements and the use of common-centroid differential amplifiers reduce some variations, but a size increase does not always suffice. Also, bandwidth decreases due to the larger junction capacitance, or you must use higher currents to retain bandwidth.

To avoid these problems, you can frequently compensate for process variances with calibration and alignment circuits. Many techniques are available for offset, gain, and operating-point adjustment. These techniques include dynamic calibration, static calibration under digital control, and static calibration during testing.

An example of dynamic calibration is an ac-coupled clocked comparator with the voltage on the coupling capacitors canceling the comparator offset. When the comparator is in precharge mode, the capacitors' inputs connect to a common voltage, and outputs are fed back to drive the coupling capacitors (Figure 6a). This

approach forces the inputs to the comparator's crossover point. The capacitors charge up to the offset voltage. When the comparator is in compare mode, the input connects to the comparator through a capacitor voltage that cancels the input offset voltage (Figure 6b). This approach provides an offset-free comparator.

In static calibration under digital control, circuits go through a digitally controlled alignment process for compensation. This alignment typically happens at circuit power-up or under host process control.

The circuits store calibration control and maintain the value while the linear circuit is in use. You can apply this type of system to compensate for offsets, gain variance, and current-source matching. You can use digital-system control to compensate for the limitations of analog-CMOS devices.

Dynamic calibration and static calibration under digital control can compensate for many process variations. The techniques are comparative and are frequently sufficient. However, some systems require calibration during production testing. In this method, digital control from the IC tester determines the proper digital pattern for a calibrated circuit. This pattern then requires permanent storage in the IC. The IC tester can force a voltage that opens small-geometry fuses. The resulting high current opens a fuse link. You can also use lasers to open fuse links. This process of "link blowing" allows permanent adjustments while the circuit is on the test system. Linear laser trimming is not as cost-effective in high-volume production. Also, many other alignment and calibration methods exist (references 2, 3, and 4).

Note that the wide parameter variance of CMOS frequently requires alignment and calibration circuitry to produce accurate and consistent functions.

LAYOUT AND MASK DESIGN

You can achieve additional noise isolation in metal-mask design through the judicious use of shielding. Using metal-

layer shields around analog signals is effective. For example, you can use a shield on all sides that is electrically connected by vias and grounded (Figure 7).

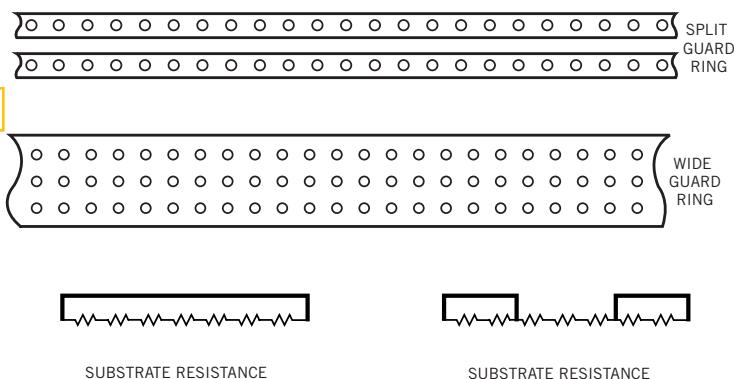
Passing a signal as a shielded differential pair can lower the effects of common-mode noise and variations between local grounds. You should optimize noise isolation at the receiver. For this reason, you should connect the shield to a ground reference at the receiver only. Shielding a nondifferential signal means that the signal is still susceptible to ground noise.

Substrate coupling is common to all elements of an IC die. Noise transients generated in digital areas are present across the chip. For P-substrate, N-well CMOS, guard rings consist of connections to both ground and power. A grounded guard ring uses a low-resistance P+ area to connect to ground (Figure 8). A guard ring that connects to the power uses an N-well and N+ region on the substrate with the goal of providing two stable, noise-free connections that help reduce noise coupling through the substrate. Positive N+ connection attracts electrons, and the grounded P+ connection attracts holes. The guard ring attempts to provide a barrier to noise coupling. You must place guard rings close to the noise source and around the “receiver” circuits, which need noise shielding. The effect is reduced noise from the source and at the receiver.

A grounded guard ring at the receiver somewhat helps noise and ground stability, but dual rings with the distributed resistance of the substrate between rings works better. The double-ring structure allows noise shielding, but noise couples to the second ring only through the resistance of the substrate (Figure 9). These rings are an imperfect approach, however. The rings typically measure about 1 μm deep, and noise and substrate current can go under the rings.

You should group analog signals away from digital signals. Digital I/O cells generate large noise transients due to the currents necessary to drive external loads. Ground pins between digital and analog pins are desirable. Grouping logic signals also helps. Any logic signals that are near the analog pins should be static digital controls. You should isolate

Figure 9



A grounded guard ring at the receiver somewhat helps noise and ground stability, but dual rings with the distributed resistance of the substrate improve noise shielding.

clocks and high-frequency datapaths from these analog signals.

Internal filter capacitors are necessary for high-frequency noise performance. However, you can often add internal filter capacitors without affecting die size. As layout designs near completion, you should review the designs for empty areas that the design is not using and fill these areas with filter capacitors. Also, metal-layer routing takes a large amount of die space. Most capacitors reside in base layers underneath metal layers. This approach allows designers to put distributed filter capacitance underneath any area used only for metal routing.

Route power buses for distribution of power and ground on top of each other. This approach provides a power-filter capacitor between metal layers and reduces die area. Also, place a filter capacitor under the power-bus areas. Using these methods lets you include sizable power-filter capacitors without increasing the die size.

You should route logic controls from one side of the cell and analog signals from the opposite side. Further, place mixed-signal cells with the analog side of the cell beside the bonding pads that have analog signals. This technique minimizes routing of analog signals and gives less opportunity for noise coupling.

CONCLUSIONS

Process variance, noise, and model accuracy can all lead to problems with SOC designs. CMOS is unfriendly to analog design, but using digital controls for calibration and alignment can help

you avoid many problems of the limitations inherent to CMOS designs. □

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