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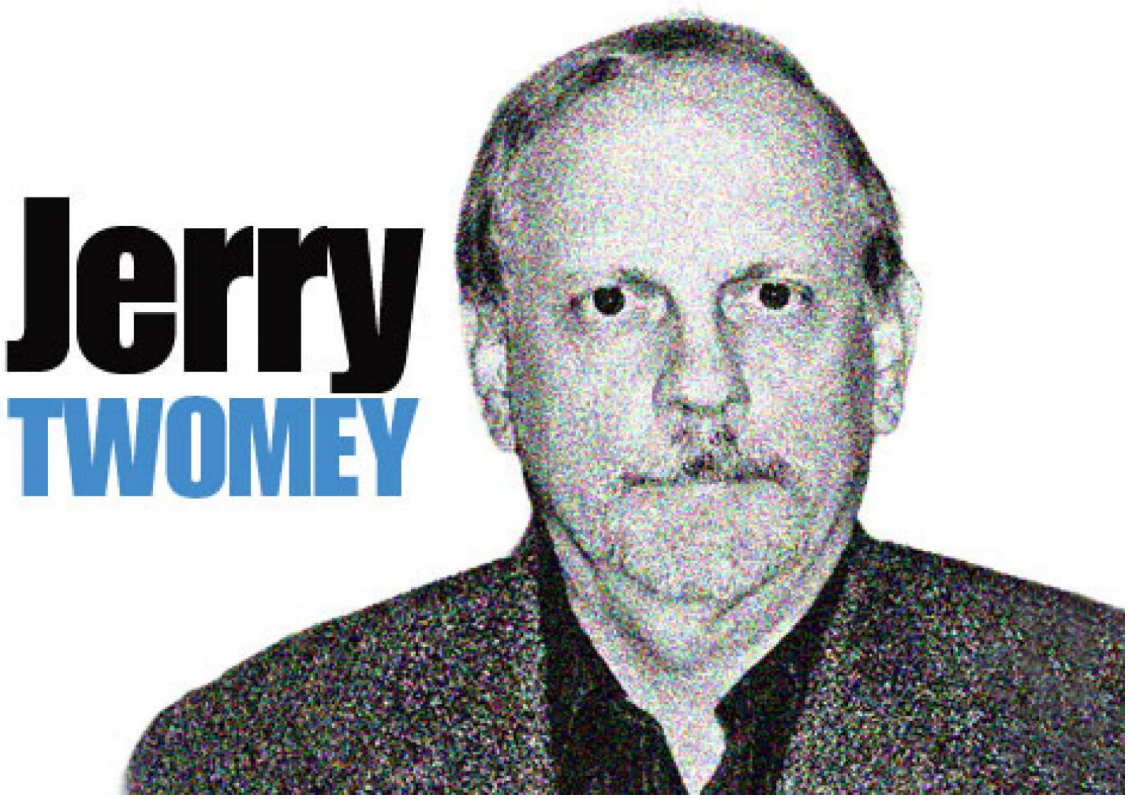

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Marketing And Technology Collide In Competitive Chip Design

Jerry Twomey | Oct 11, 2012

Every engineer needs a little marketing savvy to produce successful ICs.

Engineers tend to concentrate on the technical part of a design and ignore the other aspects of a marketable product. Frequently, designers don't understand marketing and business needs. Also,

the marketing department doesn't understand the limitations and challenges of the design process. Both need to know a little more about the other.

If you're an IC designer, you want to make sure that chip goes out the door in the millions and doesn't collect dust in the back room of some lab, long after it has failed to sell. Considering the R&D of a single IC can cost millions of dollars, it's an expensive game to play, so it's best to start with a fair shuffle of the deck.

Cost And Size Matter

All else equal, price will be the deciding point on whether your chip ends up in a product. If it meets the needs of the design, then the component engineer will generally make the final decision based on the bottom line. Admittedly, somebody involved in military or other high-margin products doesn't think along those paths, but the high-volume winners are consumer products where millions of devices are the norm. Production cost gets driven by a handful of factors, such as die/wafer cost, yield losses, packaging, and testing overhead. The elephant in the room is usually the cost of the die.

Die cost comes down to two things: die size and wafer cost. So if size matters so much, where can we reduce space? The digital parts of any chip, although large, are being optimized for gate count as part of the hardware description language (HDL) and synthesis process. Items like inductors, capacitors, and, to a lesser extent, resistors usually take up the real estate. Optimizing the design to reduce passive device area is always useful. Beyond those components, I/O cells tend to occupy a lot of area, generally due to bond pads, driver circuits, and electrostatic discharge (ESD) circuitry. Higher currents demand bigger sizes.

At the system architecture level, make an effort to reduce the number of I/O ports. Use multipurpose pins when possible, with the capability to change function under control downloads. Also, eliminate discrete external control pins where possible. Data paths should be serial (I^2C, SPI, SMB, USB) instead of parallel. It will be very unique to your design, but making this effort early in the R&D process will lead to smaller chips in most cases. Trying to do this in the architecture late in the design cycle often doesn't work.

Classic chip layouts where the core electronics are surrounded by a ring of I/O cells and bonding pads can be considered core limited or pad limited. A core-limited design has minimized the number of I/O cells and can't shrink anymore. Pad-limited designs can shrink if you can find creative ways to reduce your I/O cells.

Just Good Enough Constraint

As a general rule, your design needs to be "just good enough" to get the job done. For lack of a better way of describing it, circuit designs need to hit the requirements of the system and not much more. The cheapest functional solution generally owns the market, and "over design" tends to push up power consumption or circuit area. Unnecessarily higher power consumption leads to more expensive batteries or power supplies, and larger area leads to a higher cost per chip.

The outcome becomes a need for narrow performance specifications to produce cost-competitive designs. I have seen this applicable in RF designs, where linearity and noise well exceeded requirements at the cost of both power and size.

The design works great from the IC designer's perspective, but the component engineer selecting a device for consumer electronics will consider chip cost and power consumption. Optimal size and power consumption produces cost-effective products. System-level engineers need good communication with transistor-level designers, because a double-padded set of performance criteria results in a bloated design.

Picking Your Foundry Process

The most recent generations of silicon come at a hefty price premium. A dedicated mask set for 22 nm will cost over a million dollars, while older silicon families can be produced at considerably lower costs. Also, during the R&D phase, getting your chips done as part of a shared mask set or "multi project wafer" can help cut fabrication costs.

Cost savings can be significant using older technology, because cutting-edge silicon is only needed in the digitally intensive area of high-end multiprocessors, real-time digital graphics, and similar technologies. Many commodity ICs and even many system-on-chip (SoC) architectures can be produced efficiently on earlier generations of silicon.

The chip's interface requirements will be somewhat fitted to the CMOS generation as well. Don't expect to get 5-V I/Os when the core voltage of the device is at 1.2 V. Most CMOS families will support I/O that interfaces to a prior generation but not beyond that. Options at the foundry include metal layers, higher-quality resistors and capacitors due to polysilicon, and oxide options. All add cost, and the "nice or necessary?" question needs to be asked.

Moore's law has made process migrations part of the semiconductor business. What got implemented in 180 nm got re-designed for 130 nm, 90 nm, and so forth. Digital systems migrate at the Verilog level with some crank turning. Analog migrations require major redesign. Circuit architectures viable at 5 V and 1 µm often aren't feasible at 1 V and 45 nm.

Methods used have changed from one CMOS generation to the next. Determine if the chip will be a candidate for process migration and what steps can be taken to make the device migration friendly. Many vendors produce chipsets where the digital migrates forward while the analog side remains on an earlier generation of silicon. This has been a successful strategy.

Making The Market Window

Chips get developed to fit an emerging market need. Wi-Fi, Bluetooth, ZigBee, and 3G/4G/LTE cellular all required compliant devices with early introduction times. Market success requires quick time-to-market and cost-competitive designs. Keep it small and deliver it early to make your market window.

Emerging market designs need a timeline strategy for front-of-the-line execution. If it's an emerging standard, you need to be involved in developing it. In many cases, you can develop your chipset as the standard details are still being defined. If you wait until the standard is finalized to develop your design, then you're already too late.

Many Wi-Fi startups tried to develop chip sets. Those that didn't meet the early market window didn't survive for a second-generation product. Some late-to-market vendors got some market

share after introducing smaller designs where they could seriously undercut the costs of their competitors. However, profit margins on those chips were slashed to create those sales. It's one of many examples where cost and time-to-market lead the Darwinism of semiconductor evolution.

Sources And Targets

The "Not Invented Here" force can be very strong with some design teams. But since time-to-market is so important for some SoC development, sometimes finding alternative sources for intellectual property (IP) may be necessary. It's unique to the problem at hand and the resources available. Don't dismiss the possibility of using alternative IP sources if needed to meet the time schedule. Royalty costs for the analog-to-digital converter (ADC) or phase-locked loop (PLL) may seem small in comparison to zero sales because you're late to market.

Designing for a limited audience or a single customer carries a high risk-reward tradeoff. It's a guaranteed market, but there are a lot of business risks. Certain markets require a very tight relationship between the chip designer and the final product the chip is used in. Either the market evolves quickly or is so user specific that a direct interface between chip and system designers is the only path to a viable product. This is especially true in areas where an industry standard doesn't exist.

Products designed to satisfy industry standards enjoy the benefit of longer life spans and a well-defined target product. However, multiple design houses invariably will try to fit that standard. Low cost and early time-to-market can yield success. But due to the multi-source nature of the product, profit margins on products get minimized as more sources come to market.

A chip or chipset with a limited life span creates multiple challenges. There are the usual challenges of cost and time-to-market, as well as the added complication of the limited life of the design. This can vary by application and product life. For example, there was a huge but brief market for digital converters used for analog televisions when the Federal Communications Commission dropped analog TV broadcasts, with the market quickly dying as legacy televisions became equipped.

The SoC has allowed board-level system design to become very modular. As a result, OEMs are looking for chipsets that will provide end-to-end solutions. Depending on your product, it can be a single-chip or multi-chip solution. If end-to-end solutions are the norm, don't try to develop a piece of the system because it won't sell. Smaller organizations in the past have collaborated to produce chipset solutions coming from multiple vendors with limited success, but you need to offer a total solution.

What Makes Your IC Special?

Commodity designs like standard gate logic, stock microcontrollers, op amps, and power management devices have multiple vendors with extensive product offerings. If you compete in this space, the important question is what makes the device unique. Cost savings is the most compelling factor that will allow you to succeed, but still, it's no guarantee. You also could integrate devices that are frequently used together but only exist independently. If you can reduce the solution cost and it doesn't exist elsewhere, you may have a product with potential.

Convenience is another factor that can help a vendor succeed. Easily used documentation, clearly developed application notes, reference designs, and well explained design examples all will help

sell an IC. Board-level designers will toss aside poor documentation and use another source. They want the printed-circuit board (PCB) to work up on the first try without looking foolish. Some vendors have taken that to the next level and automated the design process with online development tools to ease utilization. Digital devices such as FPGAs, complex programmable logic devices (CPLDs), and microcontrollers require a quality integrated design environment (IDE) to be considered.

Conclusions

The semiconductor industry has many different specialties when it comes to chip architectures that sell in volume. Success in high-volume markets requires low costs, fast time-to-market, and complete solutions that are easily utilized. Get these factors right, and you stand a chance. Get them wrong, and you're history. It's a high-stakes game where you need millions of dollars to sit at the table. Don't play with the deck stacked against you.