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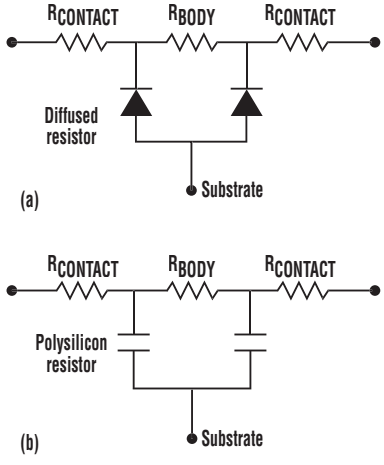
Simulation Vs. Silicon: Avoid Costly Mistakes With Accurate Models

When first-pass silicon arrives back from the foundry, accurate simulation models are critical to first-time success.

Of course, we all prefer to avoid expensive learning experiences. So every designer's ultimate goal is to hear the response "first-time functional!"

Fabricating an IC is costly, and foundry time can be as long as four months. So it's key to get it right the first time, because this saves both time and money. Yes, the EDA industry provides powerful tools for circuit design. But these tools can either expedite your design or produce results that have little or nothing to do with the actual silicon.

Most "broken silicon" has resulted from interference noise not being addressed or the model not accurately representing the silicon. Analog designs, including mixed-signal and RF chips, cause the most problems. By taking an analytical look at simulation setup, you can gain a better understanding of how to properly model a circuit. After improving the model, simulation results become quite similar to silicon.



1. Composite models for resistors can include parasitic diodes (a) or capacitors (b). $R_{CONTACT}$ represents the connection between the body and the metal layers.

Modern EDA tools have resolved the issues associated with the equations of electronics. But frequently, the model is incomplete, doesn't represent the component properly, or has some other limitation. Items like parasitic elements, process variance, element mismatch, inaccurate primitive models, implicit components left out of simulations, operating conditions, and modes of operation must be examined.

Also, simulations generally don't reveal coupling of digital switching transients to analog signals, capacitive/electromagnetic coupling, and substrate noise. Interference noise won't be shown unless the noise paths are defined in the model. This has to be addressed during all design stages: architecture, circuit design, and layout.[1] Particular areas to be investigated include:

Primitive element models: Designers must examine foundry-supplied models, including resistors, capacitors, inductors, interconnect metals, and semiconductors. They need to determine the limitations and accuracy of these models with respect to their circuits. RF design will be sensitive to parasitic capacitance and interconnect inductance. Power electronics will have to address issues with high currents and thermal gradients. Frequently, foundry models don't represent specific design scenarios.

Functional block configuration: Circuit simulation must include the elements that will be present in a final application, such as input impedance, package models, output loading, and power/ground impedances.

Simulator limitations and common pitfalls: Simulators are tools. A properly used tool aids productivity. But any tool can be used improperly, causing problems. Also, some limitations inherent to simulators and how designers configure them must be looked at.

Circuit architecture and test cases: Functional circuits under nominal conditions are the first step. But corner testing, mismatch, offsets, linearity, specifics of the application, and other areas require examination as well.

PRIMITIVE ELEMENT MODELS • A meticulous review of both passive and transistor models is necessary for design success. That means understanding models, their parameters, and how they were derived. Blind acceptance of the model set isn't a wise course of action. In fact, recent designs in a state-of-the-art CMOS process revealed some serious model deficiencies.

Also, models vary greatly in quality. At one extreme, models can represent statistical data from multiple foundry cycles. Every parasitic can be accounted for; thermal effects, breakdowns, and variance mismatch can be included as part of a composite structure ready for use in simulation.

But some models might be developed before the foundry ever produces a single wafer. Simulations of the physical foundry process are used to define a physical model of the elements. Then, the electrical model parameters are extracted from this physical definition. Both methods are used, with a tradeoff

between accuracy and execution time. Examining the supporting data employed in model creation will quickly reveal the method used and how well it represents the process. Therefore, full data disclosure of models and how they were created becomes a foundation for the entire design. Frequently, foundry models do require improvements.

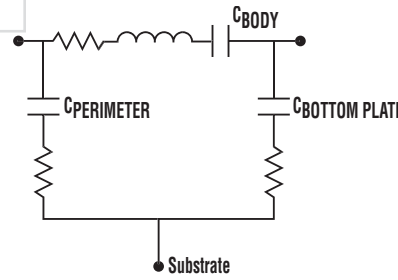
Models are usually designed for a limited set of voltages and currents, a defined temperature range, and other factors. Poorly specified items include element mismatch, noise parameters, substrate diodes, indications of excess voltages, punch-through in FETs, breakdown of PN junctions, and other "large-signal" effects. This can result in a properly functioning model—as long as the design stays within the defined constraints.

Under certain conditions, however, the model may no longer represent the application. If devices lie outside of typical operating range, examining curve-tracer data for the actual elements is suggested. This, along with inspection of the simulation models, should indicate the model's limitations. If the model is nonfunctional under some conditions, it should have warnings that occur when running the simulation.

Composite models that include parasitics, and anything associated with the "on silicon" element, are preferred. Manually adding substrate diodes, contact resistance, and other factors is prone to error and should be avoided. Figure 1 shows a composite resistor model. R_{BODY} will usually be a function of width, length, temperature, process variance, and bias voltage. $R_{CONTACT}$ represents the connection between the body and the metal layers.

Size restrictions should reflect limitations of the foundry process. The third wire represents the substrate. Diffused resistors will include parasitic diodes that are usually back-biased *(Fig. 1a)*. Also required are parasitic capacitances, both perimeter and area, as a function of operating point *(Fig. 1b)*. Higher-frequency models may incorporate more reactive elements. And, micropower models should include current leakage from resistor to substrate.

Figure 2 shows a composite capacitor model. The bottom plate to substrate, and perimeter of the top plate to substrate, must be represented. Some cases may require current leakage between



2. Composite models for capacitors need to account for the parasitics between the substrate and the bottom plate, plus the substrate and the perimeter of the top plate.

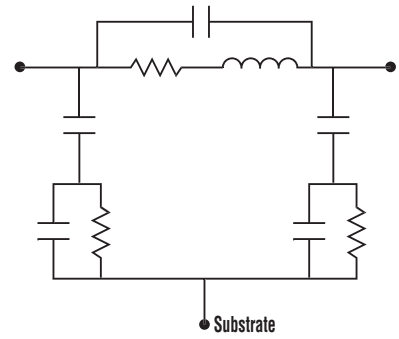
plates as well as the distributed plate impedance. Size restrictions should be placed when needed. If a MOSFET is used as a capacitor, the transistor model will generally suffice.

Figure 3 details a composite model of a planar spiral inductor. A series resistance defines the inductor's quality factor. More exact network models are available from electromagnetic simulations based on the physical definition.

There are two aspects to transistor simulation—model limitations and inaccuracies of model parameters. One issue is the equation set, and the other is the numbers put into the equations.

MOSFET models are predominantly from the Device Research Group at the University of California, Berkeley. As of October 2004, BSIM 4.4.0 is the most up to date, but revisions are always ongoing. Check out *www.device.eecs.berkeley.edu/~bim3* for information on model limitations.

Bipolar models come from several different sources. Information on these



3. This composite model for a planar spiral inductor uses a series resistance to define the quality factor. Also shown are the parasitic effects between the inductor and the substrate.

models can be found on the Compact Model Council site at *www.eigroup.org*. Also, the quick evolution of silicon causes transistor models to lag foundry processes. Higher frequencies, smaller geometry, and thinner dielectrics all lead to an ongoing need for revision.

When it comes to modeling transistor parameters, dc-bias curve fitting is usually accurate due to easy measurement and models being valid over a limited size range. Beyond that, it depends on the efforts of the model development team. Some common problem areas leading to inaccurate model parameters include:

Nonlinear capacitors: This includes reverse-biased diodes associated with drain/source to bulk or the static charge associated with inverting the MOSFET channel. Accurate measurement of these parameters is difficult and often requires indirectly estimating their values.

Subthreshold and micropower parameters: Low currents, and voltages below threshold, make measuring these parameters a challenge.

Noise coefficients: Both thermal noise and low-frequency flicker noise are often poorly specified.

Capacitance and resistance associated with wells: A common example is the n-well under a PMOS transistor. The RC time constant associated with well charge/discharge isn't defined as part of the transistor model.

Process corner models: These are "weak/strong" or "slow/fast" models. They're sometimes done by numeric manipulation of the nominal model and don't always represent the actual foundry variance seen.

Even diode models can't be taken for granted. Again, the model quality largely depends on the effort made. Among the common problems are:

Accuracy of nonlinear capacitors: The junction depletion capacitance is often inaccurate.

Flicker-noise parameters: Often this isn't specified, and the default value gives a "no-flicker-noise" diode.

Lack of a transit-time parameter: If not specified, this defaults to zero and is invalid at high frequencies.

Series resistance: Either this isn't specified and defaults to zero, or is

derived from a single-size diode, which hasn't been validated over a wide geometry range.

Invalid geometry scaling: If the device has size scaling, then the model needs to remain valid for size changes.

Primitive models require other items too. A valuable addition is a set of operating-point-violation flags. With these, any model creates a simulation error message when outside the model's functional limits or violating a foundry-defined limit. This includes overvoltage, excess current, thermal limits, and similar items. If silicon is operated in a self-destructive mode or where the model isn't valid, then this should be indicated by the simulation. Frequently, such a feature doesn't exist.

FUNCTIONAL BLOCK CONFIGURATION • This includes items needed to represent the design in a final application environment. Interconnections, I/O cells, ESD protection, bond wires, package models, power/ground models, input signals, and output loads are added here.

Interconnect loading: Every connection has RLC parasitics, but trying to model every connection usually isn't practical. However, connections with high frequency, high current, or long signal paths can have appropriate models added. After layout, automated parasitic extraction tools are available to back-annotate these into a simulation. ESD and I/O circuits present significant loads due to their large size.

Package and bond-wire models: This becomes important at high frequencies. In addition to series impedance, these models provide information about signals coupled between pins. Any two pins will have magnetic and capacitive coupling between them. A package model frequently shows that a digital signal coming into the chip is coupling over to some analog input.

Input signals: Input signals aren't ideal. Amplitude modulation, interference noise, wideband white noise, harmonic distortion, and source impedance are present and must be included.

Power and ground: External power and ground demand the appropriate series impedance. And, external power-supply capacitors require modeling of their inherent series inductance so that the frequency response is accurate. Transient loads should produce some variance in power and ground.

Appropriate output loads: Resistive or capacitive loads will affect gain and bandwidth. Inductive loads may need special consideration for voltage transients outside the power/ground rails.

SIMULATOR LIMITATIONS AND COMMON PITFALLS • It's more common for the models to be in error, rather than the simulator itself. Yet some issues are directly related to the simulator.

Berkeley Spice: The original Spice was developed at the University of California at Berkeley, with several different versions released between 1971 and 1983. Due to open-source availability, a number of commercial tools use various versions of this software. However, it has limitations that make an unmodified version difficult to use in commercial product development.

Simulator time step: This affects the accuracy of the simulation output and can hide high-frequency issues. Manual inspection can give an approximate circuit bandwidth, and an appropriate time step can be selected. Newer simulation tools do this automatically.

Error-tolerance definition: Simulators resolve circuits to a defined limit of accuracy, as selected by the user. If improperly set, the results are inaccurate. This is seen in current summation, or series voltage addition with widely different values.

Integration type: Simulators perform integration by a numerical approximation method. Some of the algorithms used can hide instabilities, while others can enhance them. Because of this difference, most simulation tools can select the integration method used. If several different integration methods produce similar results, "integration type" can probably be eliminated as an issue.

CIRCUIT ARCHITECTURE AND TEST CASES • Several items frequently get overlooked, rendering a chip nonfunctional:

Need for absolute component value accuracy: A 20% process variance from nominal component value isn't unusual. The foundry can provide specific data here. Wherever possible, circuits that don't rely on accurate compo-

nents are preferred.

Dependence on matched elements: It's not easy to get two resistors of precisely the same value, a differential pair of transistors without any offset, or 10 current sources producing the exact same current. Foundry-available "matching data" will show what's viable. Introducing mismatch and offsets as appropriate should be part of the simulations.

Sensitive phase relationships: The phase relationship of signals, switches opening/closing, and other event sequences requires examination. Exact time alignment will change with process, voltage, and temperature. Robust designs should be insensitive to these effects.

Top-level simulation: The total chip simulation may be different than simulation of its individual parts. Loading changes gains and operating points. Control-signal polarity may be inverted. Transients in one circuit may corrupt the power in another. Validation of interconnect by a simulator also helps reduce human error factors.

Stability of feedback systems: Feedback systems functioning without oscillation or ringing under nominal conditions are the first step. A quantitative stability analysis (with gain and phase margins) over the design variables will prevent the device from becoming unusable in process corners.

Problem-free power cycling: Power supplies don't always turn on cleanly. Designers have to consider transient voltages while power-supply capacitors charge/discharge, brief power dropouts, and mechanical switches that produce "glitchy" power due to contact bounce. Hot plugging, multiple power supplies turning on at different times, and control signals changing unexpectedly also need attention. In addition, definition must be applied to power cycle-time limits and what the device does during the power cycle. The ultimate goal is a nondestructive system and predictable on-off cycle, no matter what happens outside the chip.

Noise analysis: Inherent noise (flicker and thermal noise being best known) isn't shown in most transient simulations. However, EDA tools can perform specific tests for quantitative information on noise performance. All non-ideal circuit elements produce noise. So if it seems noiseless, then the model didn't include the needed noise parameters and the default is noise-free.

Linearity and dynamic range: Nobody wants an amplifier clipping or producing spectral harmonics. But ac analysis is "small signal" and will not show linearity problems. These will be seen in transient simulations. A combination of minimum power-supply voltage, largest input signals, maximum gain settings, or similar conditions may show nonlinear response problems.

Process, voltage, temperature (PVT) simulations: Variations in PVT are typical for corner tests. For every parameter (e.g., weak/strong NMOS, high/low polysilicon resistance), the number of simulations double and thus may require a large number of simulations. Also, for high temperatures, the thermal elevation due to power consumed inside the IC is needed.

A good design requires a good layout: A detailed discussion of layout techniques has been presented elsewhere.[2] Care in the placement of matched elements, signal paths, shielding, and many other issues all require careful attention. Layout quality can strongly affect design performance.

So when you hear, "But the simulations work okay," remember that the end result is silicon and not simulation outputs. Simulating a design with confidence that the actual chip will perform in a similar fashion is the start of a successful design. Getting a chip that plugs and plays properly is the final goal.

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